meet a target transconductance (g_m) versus gate-to-source voltage (Vgs) curve for the thin film transistor.

29. (canceled)

30. The semiconductor device of claim **1**, wherein the second body region has a thickness as measured between the first body region and the third body region of between 50 to 80 nanometers.

31. The semiconductor device of claim **1**, wherein the second body region has a thickness as measured between the first body region and the third body region of between 80 to 120 nanometers.

32. A method of forming a semiconductor device, comprising:

forming a first conductive line above a semiconductor substrate having a major surface that extends in a horizontal plane;

forming a thin film transistor comprising:

i) forming a first semiconductor layer having a first peak doping concentration of a first type of conductivity, including forming the first semiconductor layer in electrical contact with the first conductive line;

ii) forming a second semiconductor layer having a second peak doping concentration of a second type of conductivity that is opposite the first type of conductivity;

iii) forming a third semiconductor layer having a third peak doping concentration of the first type of conductivity, wherein the third semiconductor layer has a thickness of between 50 to 120 nanometers;

iv) forming a fourth semiconductor layer having a fourth peak doping concentration of the second type of conductivity;

v) forming a fifth semiconductor layer having a fifth peak doping concentration of the first type of conductivity, wherein the first, second, third, fourth, and fifth semiconductor layers form a stack that extends in the vertical direction, wherein the first, third and fifth peak doping concentrations are each at least 10 times greater than the second peak doping concentration and at least 10 times greater than the fourth peak doping concentration;

vi) forming a tunnel dielectric as a conformal layer on the first, second, third, fourth, and fifth semiconductor layers; and

vii) forming a conductive control gate adjacent to the second, third, and fourth semiconductor layers, wherein the tunnel dielectric is between the conductive control gate and the second, third, and fourth semiconductor layers; and

forming a second conductive line that extends in a vertical direction with respect to the horizontal plane, including forming the second conductive line in electrical contact with the fifth semiconductor layer.

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